AMENDMENTS TO THE SPECIFICATION

IN THE SPECIFICATION:

Please amend the paragraph bridging pages 5 and 6 as follows:

-- The pulse output module 20 outputs a programmable pulse signal to control a controlled system such as a servo motor. As shown in FIG. 3, the pulse output module 20 mainly contains a pulse output starting module 21 for outputting a start signal to start a PWM module 22, a PLSY module 23, or a PLSR module 24. The started module then outputs the corresponding pulse signal through a multiplexer~~de-multiplexier~~ 25. The PWM module performs pulse width modulation. The PLSY module outputs pulses. The PLSR module outputs speed-reduced pulses. They are all used to control motors. One can have different settings according to different motor driving means.--

Please amend the paragraph bridging pages 8 and 9 as follows:

-- The counting module 40 contains a counter comparison value recording unit 41 and a counter current value recording unit 42, storing a counter comparison value and a counter current value, respectively. A counting comparison unit 43 compares the counter comparison value and the counter current value. When the former value (U value) is reached, a logic 1 is output to the ~~de-multiplexier~~ de-multiplexer 44. When the latter value (D value) is reached, a logic 0 is output to the ~~de-multiplexier~~de-multiplexer 44. The ~~de-multiplexier~~de-multiplexer 44 uses the counting mode to output a signal to the basic command executing module 10.--

Please amend the paragraph beginning page 9, line 3 as follows:

-- The counter current value recording unit 42 uses the outputs from the ~~de-multiplexier~~de-multiplexer 45A, the multiplexer~~multiplexier~~ 45B ~~and~~, the ~~de-multiplexier~~ de-multiplexer ~~45B~~46A, the multiplexer~~de-multiplexier~~ 46B to output the counter current value to a Up/Down counting detecting unit 47 to detect whether the current counting is upward counting or downward counting. If it is upward counting, a logic 0 is output to the ~~de-multiplexier~~de-multiplexer 48. If it is downward counting, a logic 1 is output to the ~~de-multiplexier~~de-multiplexer 48. The ~~de-multiplexier~~de-multiplexer 48 follows the counting mode to output the signal to the basic command executing module 10.--

Please amend the paragraph beginning page 9, line 11 as follows:

-- The counter current value unit 42 further outputs a counting content signal to a multiplexer~~multiplexier~~ 54. The counter current value unit 42 is controlled by three control signals: a reset signal, a start signal, and a U/D flag. The reset signal is output from an AND logic operation unit 49A. The start signal is output from an AND logic operation unit 49B.--

Please amend the paragraph bridging pages 9 and 10 as follows:

-- With reference to FIG. 8, the counting comparison module 50 contains a comparison result output address unit 51, a comparison mode setting unit 52, and a

counting comparison setting value unit 53. The comparison result output address unit 51 stores comparison result output addresses. The comparison mode setting unit 52 stores comparison mode settings. The counting comparison setting value unit 53 stores counting comparison setting values. The multiplexer~~de-multiplexier~~ 54 receives four output signals (HSC0, HSC1, HSC2, HSC3) from the counter for outputting a counting content. A sixth comparator 55 compares the counting content and the counting comparison value settings, and outputs the comparison result to a ~~multiplexier~~ de-multiplexer 57 and a multiplexer~~de-multiplexier~~ 58. The de-multiplexer~~multiplexier~~ 57 and the multiplexer~~de-multiplexier~~ 58 outputs the operation results to the basic command executing module 10. Another comparison result of the sixth comparator 55 is output and stored in a comparison result buffer 56.--